In re Patent Application of:
ROCHE ET AL.
Serial No. **09/995,251**
Filing Date: **NOVEMBER 27, 2001**

In the Claims:

Claims 1 to 14 (Cancelled).

15. (Previously Presented) A microprocessor comprising:

a first terminal for receiving a mode selection signal;

a second terminal for receiving a control signal; and

selection means connected to the first and second terminals for selecting an operating mode of the microprocessor based upon the mode selection signal and the control signal, said selection means comprising

a counter having a counting input and a reset input,

first coupling means coupling the counting input to the first terminal,

second coupling means coupling the reset input to the second terminal, and

default means for maintaining by default the reset input at a first logic value for ensuring that said counter is maintained at zero in an absence of the control signal.

16. (Previously Presented) A microprocessor according to Claim 15, wherein said default means is internal to the microprocessor.

17. (Previously Presented) A microprocessor according to Claim 15, wherein said default means is external

to the microprocessor.

18. (Previously Presented) A microprocessor according to Claim 15, wherein said default means comprises a bias resistor.

19. (Previously Presented) A microprocessor according to Claim 15, wherein said second coupling means comprises a second logic circuit having an output coupled to the reset input of said counter, a first input coupled to the second terminal, and a second input for receiving an inhibit signal for inhibiting the output of the said second logic circuit when the first input receives the control signal outside a selection period for selecting an operating mode of the microprocessor.

20. (Previously Presented) A microprocessor according to Claim 19, wherein the inhibit signal is a reset signal of the microprocessor.

21. (Previously Presented) A microprocessor according to Claim 20, wherein said second logic circuit comprises:

an invertor having an input for receiving the reset signal; and

an AND-gate having a first input connected to the second terminal, and a second input connected to an output of said invertor.

22. (Previously Presented) A microprocessor

according to Claim 15, further comprising:

a decoder connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter; and

a central processing unit connected to an output of said decoder for receiving the at least one mode bit.

23. (Previously Presented) A microprocessor according to Claim 15, wherein said first coupling means comprises a first logic circuit having an output coupled to the counting input of said counter, a first input coupled to the first terminal, and a second input for receiving an inhibit signal for inhibiting the output of the said first logic circuit when the first input receives the mode selection signal outside a selection period for selecting an operating mode of the microprocessor.

24. (Previously Presented) A microprocessor according to Claim 15, wherein the operating mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the operating mode of the microprocessor.

25. (Previously Presented) A microprocessor according to Claim 15, wherein the first and the second terminals are used as input/output ports of the microprocessor when the microprocessor is operating outside a selection period for selecting the operating mode thereof.

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26. (Previously Presented) A microprocessor comprising:

a first terminal for receiving a mode selection signal;

a second terminal for receiving a control signal; and

a selection circuit connected to the first and second terminals for selecting a mode of the microprocessor based upon the mode selection signal and the control signal, said selection circuit comprising

a counter having a counting input and a reset input,

a first coupling circuit coupling the counting input to the first terminal,

a second coupling circuit coupling the reset input to the second terminal, and

a device for maintaining the reset input at a first logic value for ensuring that said counter is maintained at a predetermined value in an absence of the control signal.

27. (Previously Presented) A microprocessor according to Claim 26, wherein said device comprises a bias resistor connected internal to the microprocessor.

28. (Previously Presented) A microprocessor according to Claim 26, wherein said device comprises a bias resistor connected external to the microprocessor.

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29. (Previously Presented) A microprocessor according to Claim 26, wherein said second coupling circuit has an output coupled to the reset input of said counter, a first input coupled to the second terminal, and a second input for receiving an inhibit signal for inhibiting the output of the said second logic circuit when the first input receives the control signal outside a selection period for selecting a mode of the microprocessor.

30. (Previously Presented) A microprocessor according to Claim 29, wherein the inhibit signal is a reset signal of the microprocessor.

31. (Previously Presented) A microprocessor according to Claim 30, wherein said second coupling circuit comprises:

an invertor having an input for receiving the reset signal; and

an AND-gate having a first input connected to the second terminal, and a second input connected to an output of said invertor.

32. (Previously Presented) A microprocessor according to Claim 26, further comprising:

a decoder connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter; and

a central processing unit connected to an output of said decoder for receiving the at least one mode bit.

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33. (Previously Presented) A microprocessor according to Claim 26, wherein said first coupling circuit comprises a first logic circuit having an output coupled to the counting input of said counter, a first input coupled to the first terminal, and a second input for receiving an inhibit signal for inhibiting the output of the said first coupling circuit when the first input receives the mode selection signal outside a selection period for selecting a mode of the microprocessor.

34. (Previously Presented) A microprocessor according to Claim 26, wherein the mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the mode of the microprocessor.

35. (Previously Presented) A microprocessor according to Claim 26, wherein the first and the second terminals are used as input/output ports of the microprocessor when the microprocessor is operating outside a selection period for selecting the mode thereof.

36. (Previously Presented) A method for selecting an operating mode of a microprocessor comprising a counter having a counting input and a reset input, and a first coupling circuit coupling the counting input to a first terminal of the microprocessor, and a second coupling circuit coupling the reset input to a second terminal of the microprocessor, the method comprising:

driving the counting input with a mode selection signal applied to the first terminal of the microprocessor;

driving the reset input by a control signal applied to the second terminal for activating the counter; and

maintaining by default the reset input at a first logic value for ensuring that the counter is maintained at a predetermined value in an absence of the control signal.

37. (Previously Presented) A method according to Claim 36, wherein the maintaining by default is accomplished using a bias resistor internal to the microprocessor.

38. (Previously Presented) A method according to Claim 36, wherein the maintaining by default is accomplished using a bias resistor external to the microprocessor.

39. (Previously Presented) A method according to Claim 36, wherein the second coupling circuit has an output coupled to the reset input of the counter, a first input coupled to the second terminal, and a second input; the method further comprising applying an inhibit signal to the second input for inhibiting the output of the second logic circuit when the first input receives the control signal outside a selection period for selecting an operating mode of the microprocessor.

40. (Previously Presented) A method according to Claim 39, wherein the inhibit signal is a reset signal of the microprocessor.

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41. (Previously Presented) A method according to Claim 36, wherein the mode selection signal includes a predetermined number of pulses; the further comprising:

using the counter for counting the number of pulses in the mode selection signal;

generating at least one mode bit based upon the number of pulses counted; and

delivering the at least one mode bit to a central processing unit.

42. (Previously Presented) A method according to Claim 36, wherein the first coupling circuit has an output coupled to the counting input of the counter, a first input coupled to the first terminal, and a second input; the method further comprising applying an inhibit signal to the second input for inhibiting the output of the first coupling circuit when the first input receives the mode selection signal outside a selection period for selecting an operating mode of the microprocessor.

43. (Previously Presented) A method according to Claim 36, wherein the operating mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of the counter during a selection period for selecting the operating mode of the microprocessor.

44. (Previously Presented) A method according to Claim 36, wherein the first and the second terminals are used as input/output ports of the microprocessor when the

microprocessor is operating outside a selection period for selecting the operating mode thereof.

45. (New) A microprocessor comprising:

a first terminal for receiving a mode selection signal;

a second terminal for receiving a control signal; and

a selection circuit connected to the first and second terminals for selecting a mode of the microprocessor based upon the mode selection signal and the control signal, said selection circuit comprising

a counter having a counting input and a reset input,

a first coupling circuit coupling the counting input to the first terminal, and comprising

a first logic circuit having an output coupled to the counting input of said counter,

a first input coupled to the first terminal, and

a second input for receiving an inhibit signal for inhibiting the output of the said first coupling circuit when the first input receives the mode selection signal outside a selection period for selecting a mode of the microprocessor, and

a second coupling circuit coupling the reset input to the second terminal, and

a device for maintaining the reset input at a first logic value for ensuring that said counter is maintained at a predetermined value in an absence of

the control signal.

46. (New) A microprocessor according to Claim 45, wherein said device comprises a bias resistor connected internal to the microprocessor.

47. (New) A microprocessor according to Claim 45, wherein said device comprises a bias resistor connected external to the microprocessor.

48. (New) A microprocessor according to Claim 45, wherein said second coupling circuit has an output coupled to the reset input of said counter, a first input coupled to the second terminal, and a second input for receiving an inhibit signal for inhibiting the output of the said second logic circuit when the first input receives the control signal outside a selection period for selecting a mode of the microprocessor.

49. (New) A microprocessor according to Claim 48, wherein the inhibit signal is a reset signal of the microprocessor.

50. (New) A microprocessor according to Claim 49, wherein said second coupling circuit comprises:

an invertor having an input for receiving the reset signal; and

an AND-gate having a first input connected to the second terminal, and a second input connected to an output of said invertor.

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51. (New) A microprocessor according to Claim 45, further comprising:

a decoder connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter; and

a central processing unit connected to an output of said decoder for receiving the at least one mode bit.

52. (New) A microprocessor according to Claim 45, wherein the mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the mode of the microprocessor.

53. (New) A microprocessor according to Claim 45, wherein the first and the second terminals are used as input/output ports of the microprocessor when the microprocessor is operating outside a selection period for selecting the mode thereof.

54. (New) A microprocessor comprising:

a first terminal for receiving a mode selection signal;

a second terminal for receiving a control signal; and

a selection circuit connected to the first and second terminals for selecting a mode of the microprocessor based upon the mode selection signal and the control signal,

said selection circuit comprising

a counter having a counting input and a reset input,

a first coupling circuit coupling the counting input to the first terminal,

a second coupling circuit coupling the reset input to the second terminal, and comprising

an output coupled to the reset input of said counter,

a first input coupled to the second terminal, and

a second input for receiving an inhibit signal for inhibiting the output of the said second logic circuit when the first input receives the control signal outside a selection period for selecting a mode of the microprocessor, and

a device for maintaining the reset input at a first logic value for ensuring that said counter is maintained at a predetermined value in an absence of the control signal.

55. (New) A microprocessor according to Claim 54, wherein said device comprises a bias resistor connected internal to the microprocessor.

56. (New) A microprocessor according to Claim 54, wherein said device comprises a bias resistor connected external to the microprocessor.

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57. (New) A microprocessor according to Claim 54, wherein the inhibit signal is a reset signal of the microprocessor.

58. (New) A microprocessor according to Claim 57, wherein said second coupling circuit comprises:

an invertor having an input for receiving the reset signal; and

an AND-gate having a first input connected to the second terminal, and a second input connected to an output of said invertor.

59. (New) A microprocessor according to Claim 54, further comprising:

a decoder connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter; and

a central processing unit connected to an output of said decoder for receiving the at least one mode bit.

60. (New) A microprocessor according to Claim 54, wherein said first coupling circuit comprises a first logic circuit having an output coupled to the counting input of said counter, a first input coupled to the first terminal, and a second input for receiving an inhibit signal for inhibiting the output of the said first coupling circuit when the first input receives the mode selection signal outside a selection period for selecting a mode of the microprocessor.

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61. (New) A microprocessor according to Claim 54, wherein the mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the mode of the microprocessor.

62. (New) A microprocessor according to Claim 54, wherein the first and the second terminals are used as input/output ports of the microprocessor when the microprocessor is operating outside a selection period for selecting the mode thereof.